WHAT IS CLAIMED IS:

1. A data storage device comprising a cross point array of resistive memory elements and a plurality of blocking elements, the memory elements and the blocking elements arranged in groups, each group including series-connected memory elements and a blocking element.

2. The device of claim 1, wherein the memory elements include magnetoresistive elements.

3. The device of claim 1, wherein the memory elements include tunneling magnetoresistive elements.

4. The device of claim 1, wherein the blocking elements include diodes.

5. The device of claim 1, wherein the blocking elements include transistors.

6. The device of claim 1, further comprising a substrate, the blocking elements formed on the substrate.

7. The device of claim 1, wherein each group includes a discontinuous conductor for connecting the memory elements and the blocking element in series.

8. The device of claim 7, further comprising a plurality of first and second read lines, the first read lines being orthogonal to the second read lines, each group connected between one of the first read lines and one of the second read lines.

9. The device of claim 8, further comprising a circuit for applying a first potential to a selected first read line, and a second potential to a selected second read line during a read operation on a selected memory element, a difference between the first and second potentials causing a sense current to flow through a group including the selected memory element.

10. The device of claim 9, wherein the circuit also applies a third potential to unselected first read lines during read operations, the third potential equal to or greater than the first and second potentials, whereby sneak path currents are blocked.

11. The device of claim 9, wherein one of the first and second potentials is $V_{DD}$.

12. The device of claim 8, further comprising a plurality of first and second write lines, the first write lines orthogonal to the second write lines, each memory element at the cross point of a first write line and a second write line.

13. The device of claim 1, further comprising a circuit for performing destructive read operations on the memory elements.

14. The device of claim 1, further comprising a circuit for determining a logic value stored in a selected memory element of a selected group, the circuit causing a sense current to flow through the selected group, sampling the sense current and storing the sampled value, writing a logic value to the selected memory element in the selected group, causing a sense current to flow through the selected group, and sampling the sense current and comparing the second sampled value to the stored value.

15. An MRAM device comprising:

a cross point array of tunneling magnetoresistive memory elements; and

a plurality of sneak path blocking elements;

the device arranged in groups, each group including at least two memory elements and at least one blocking device connected in series.

16. The device of claim 15, wherein the blocking elements include diodes.

17. The device of claim 15, wherein the blocking elements include transistors.

18. The device of claim 15, further comprising a substrate, the array and the blocking elements formed on the substrate.

19. The device of claim 15, wherein each group includes a discontinuous conductor for connecting the memory elements and the blocking element in series.

20. The device of claim 15, further comprising a plurality of first and second read lines, the first read lines being orthogonal to the second read lines, each group connected between one of the first read lines and one of the second read lines.

21. The device of claim 20, further comprising a circuit for applying a first potential to a selected first read line, and a second potential to a selected second read line during a read operation on a selected memory element, a difference between the first and second potentials causing a sense current to flow through a group including the selected memory element.

22. The device of claim 21, wherein the circuit also applies a third potential to unselected first read lines during read operations, the third potential equal to or greater than the first and second potentials, whereby sneak path currents are blocked.

23. The device of claim 21, wherein one of the first and second potentials is $V_{DD}$.

24. The device of claim 20, further comprising a plurality of first and second write lines, the first write lines orthogonal to the second write lines, each memory element at the cross point of a write word line and a write bit line.

25. The device of claim 15, further comprising a circuit for performing destructive read operations on the memory elements.

26. The device of claim 15, further comprising a circuit for determining a logic value stored in a selected memory element of a selected group, the circuit causing a sense current to flow through the selected group, sampling the sense current and storing the sampled value, writing a logic value to the selected memory element in the selected group, causing a sense current to flow through the selected group, and sampling the sense current and comparing the second sampled value to the stored value.

27. A method of performing a read operation on a selected memory cell among a group of series-connected magnetoresistive memory cells, the method comprising:

causing a first sense current to flow through the group;

sampling the first sense current and storing a first sampled value;

writing to the selected memory cell;

causing a second sense current to flow through the group; and

sampling the second sense current and comparing a second sampled value to the stored value.

28. The method of claim 27, further comprising blocking sneak path currents in the array while the first and second sense currents are being sampled.

29. The method of claim 27, wherein unselected cells in the group do not change resistance states during the first and second samples and are treated as common mode resistances.

30. The method of claim 27, further comprising restoring the selected memory cell to its original resistance state if the resistance state was change during the step of writing.